



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,875	02/19/2004	Shou-Lung Chen	3313-1116P	1953
2292	7590	06/30/2005	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			VU, HUNG K	
			ART UNIT	PAPER NUMBER
			2811	
DATE MAILED: 06/30/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/780,875	<b>Applicant(s)</b> CHEN ET AL.	
	<b>Examiner</b> Hung Vu	<b>Art Unit</b> 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 1-8 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-14 and 17-21 is/are rejected.
- 7) ☒ Claim(s) 15 and 16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election of Invention of Group I, Claims 9-21, in the reply filed on 06/17/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Group I, Claims 9-21, in the reply filed on 06/17/05 is acknowledged.

Claims 1-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim.

Election was made **without** traverse in the reply filed on 06/17/05.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9, 10, 12-14, 17, 18, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuo et al. (US 2002/0036338).

Matsuo et al. discloses, as shown in Figures 1A-1C and 12, a stacked package for electronic elements, comprising:

Art Unit: 2811

a substrate (BS), having a supporting surface, wherein a plurality of stud bumps (TP) are formed on the supporting surface;

an electronic element (SBB,SBA), having a plurality of vias corresponding to the stud bumps, wherein the vias are respectively aligned with the stud bumps to securely mount the electronic element on the substrate.

Regarding claims 10 and 18, Matsuo et al. discloses the material of the stud bumps is a conductive metal (solder).

Regarding claim 12 and 21, Matsuo et al. discloses the element is silicon chip, a GaAs chip, an InP chip or an epitaxily-grown chip.

Regarding claim 13, Matsuo et al. discloses the substrate is an organic substrate, a ceramic substrate, a glass substrate, a silicon substrate or a GaAs substrate.

Regarding claim 14, Matsuo et al. discloses, as shown in Figures 1A-1C and 12, a stacked packaged for electronic elements, comprising:

a substrate (BS), having a supporting surface, wherein a plurality of stud bumps (TP) are formed on the supporting surface;

a plurality of electronic elements (SBB,SBA), each having a plurality of vias corresponding to the stud bumps, wherein the vias of each electronic element are respectively

Art Unit: 2811

aligned with the stud bumps, the stud bumps being allowed to pass through the vias so as to securely mount and stack the electronic elements on the substrate.

Regarding claim 17, Matsuo et al. discloses the package further comprising a spacer (CN) between adjacent electronic elements.

3. Claims 9, 10, 13, 14, 18 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Moden et al. (PN 6,297,548).

Moden et al. discloses, as shown in Figures 1-6, a stacked package for electronic elements, comprising:

- a substrate (2), having a supporting surface, wherein a plurality of stud bumps (162) are formed on the supporting surface;

- an electronic element (100), having a plurality of vias corresponding to the stud bumps, wherein the vias are respectively aligned with the stud bumps to securely mount the electronic element on the substrate.

Regarding claims 10 and 18, Moden et al. discloses the material of the stud bumps is a conductive metal.

Regarding claims 13 and 21, Moden et al. discloses the substrate is an organic substrate, a ceramic substrate, a glass substrate (FR-4), a silicon substrate or a GaAs substrate.

Art Unit: 2811

Regarding claim 14, Moden et al. discloses, as shown in Figures 1-6, a stacked packaged for electronic elements, comprising:

a substrate (2), having a supporting surface, wherein a plurality of stud bumps (162) are formed on the supporting surface;

a plurality of electronic elements (100), each having a plurality of vias corresponding to the stud bumps, wherein the vias of each electronic element are respectively aligned with the stud bumps, the stud bumps being allowed to pass through the vias so as to securely mount and stack the electronic elements on the substrate.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al. (US 2002/0036338).

Matsuo et al. discloses all of the claimed limitations except material of the stud bumps.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Matsuo et al. having the materials as that claimed by Applicant, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

*In re Leshin*, 125 USPQ 416.

5. Claims 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden et al. (PN 6,297,548).

Moden et al. discloses all of the claimed limitations except material of the stud bumps.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Matsuo et al. having the materials as that claimed by Applicant, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

*In re Leshin*, 125 USPQ 416.

6. Claims 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden et al. (PN 6,297,548) in view of Matsuo et al. (US 2002/0036338).

Moden et al. discloses the chip is a semiconductor chip or die. Moden et al. does not disclose the chip is a silicon chip, a GaAs chip, an InP chip or an epitaxially-grown chip. However, Matsuo et al. discloses a chip (S) is a silicon chip. Note Figures 1A-1C and 12. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the chip of Moden et al. as a silicon chip, such as taught by Matsuo et al. since silicon is conventionally used as a base to form the device thereon.

*Allowable Subject Matter*

7. Claims 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is an examiner's statement of reasons for allowance:

Applicant's claims 15 and 16 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed stacked package further comprising a solder paste that is applied over exposed surfaces of the stud bumps on the topmost electronic element, the solder paste being reflowed to flow down through the vias along the stud bumps so as to securely connect the electronic elements, as recited in claim 15; the claimed stacked package further comprising a conductive glue that is applied over the stud bumps on an exposed surface of the topmost electronic element, and flows through the vias along the stud bumps so as to securely connect the electronic elements, as recited in claim 16.

*Conclusion*

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

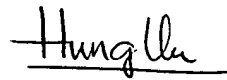


Art Unit: 2811

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

June 24, 2005

A handwritten signature in cursive script, appearing to read "Hung Vu", is written over a horizontal line.

Hung Vu

Primary Examiner